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on July 5, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: Anne Cousin Carr

PATENT
Attorney Docket No.: 015114-047930US
Client Reference No.: A293-D1

8/8
7-18-01
T. Flood

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Paul E. Brock II
Raminda U. Madurawe et al.	Art Unit: 2815
Application No.: 09/606,252	AMENDMENT
Filed: June 28, 2000	
For: HIGH VOLTAGE MOS DEVICES WITH HIGH GATED-DIODE BREAKDOWN VOLTAGE AND PUNCH-THROUGH VOLTAGE	

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Sir:

In response to the Office Action mailed January 5, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 27-28, and 35-37 as indicated below and in the attachment. Please add new claims 38-40.

Sub C1

27. (Amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate;

forming a gate oxide on the semiconductor substrate;

forming a gate on the gate oxide;